UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/707,381 | 12/09/2003 | Wen-Long Chin | ADMP0004USA | 1380 |

27765 7590 06/13/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

| EXAMINER | |
|---|---|
| HASSAN, AURANGZEB | |
| **ART UNIT** | **PAPER NUMBER** |
| 2182 | |

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/707,381 | CHIN, WEN-LONG | |
| | Examiner | Art Unit | |
| | Aurangzeb Hassan | 2182 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Azm. Fleming
FRITZ FLEMING
Supervisory PRIMARY EXAMINER 6/12/2006
GROUP 2100
AU 2181

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities: paragraph [0014] line 20 recites "the professor 24".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner is unclear as to the positive steps cited in claim 1. Line 8 of claim 1 recites input data being written. Line 11 of claim 1 recites the crypto engine reading out. Line 15 of claim 1 recites the crypto engine being written. Line 19 of claim 1 recites crypto engine reading out. Line 22 of claim 1 recites controlling the crypto engine. Line 26 of claim 1 recites controlling the buffer memory. It is suggested that the applicant clarify any and all positive steps recited in the claim.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satterfield (US Patent Number 6,125,182) in view of Lai et al (US Patent Number 6,382,846 hereinafter "Lai").

6. As per claim 1, Satterfield teaches a method for managing buffer memory, the buffer memory (I/O Buffer A and B, elements 15 and 16, figure 1) is applied to a crypto engine (figure 1), the crypto engine encrypting or decrypting an input data to produce a result through an encryption algorithm or a decryption algorithm (provides an encryption/decryption method, column 5, lines 32 – 41), the method for managing the buffer memory comprising: defining an input/output (IO) writing address in the buffer memory (defined via Address Translation Tables, element 4, figure 1, to the buffer memory address at terminals element 46a in figure 1, column 12, lines 60 – 67), the input data being written into the buffer memory beginning at the IO writing address (46a, column 22, lines 50 – 65); defining a program reading address in the buffer memory (defined via Address Translation Tables, element 4, figure 1, to the buffer memory address at terminals element 47a in figure 1, column 13, lines 13 – 18), the crypto engine reading out the input data beginning at the program reading address to process the encryption algorithm or the decryption algorithm (47a, column 22, lines 50 – 65); defining a program writing address in the buffer memory (defined via Address

Translation Tables, element 4, figure 1, to the buffer memory address at terminals element 47b in figure 1, column 13, lines 13 – 18), the result of the crypto engine being written into the buffer memory beginning at the program writing address (47b, column 22, lines 50 – 65); defining an IO reading address in the buffer memory (defined via Address Translation Tables, element 4, figure 1, to the buffer memory address at terminals element 46b in figure 1, column 12, lines 60 – 67), the crypto engine reading out the result beginning at the IO reading address and outputting the result (46b, column 22, lines 50 – 65); when the IO writing address is different from the program reading address, controlling the crypto engine to read the input data beginning at the program reading address; and when the program writing address is different from the IO reading address, controlling the buffer memory to output the result beginning at the IO reading address (figures 2a and 2b allow for determining the location of information read and written when the pointers correspond between input and output pointers along with array #1 and #2 pointers its correspondingly increments to the next location, and when different, the pointer remains at the initial beginning location previous to the controlling of the crypto engine, column 13, lines 56 – 67, column 14, lines 1 – 44, fully describe the processing of information in a buffer as applied to the two control steps listed above).

Satterfield fails to explicitly teach a method of managing a single buffer memory applied to a processing system.

Lai analogously teaches a method of managing a single buffer memory applied to a processing system (column 12, lines 32 – 44).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify Satterfield with the teachings of Lai. One of ordinary skill would have been motivated to make such modification of integrating buffer memories in order to share at least some decoding logic reducing hardware requirements (column 12, lines 32 – 44). The examiner also notes that courts have held making separate pieces integral obviousness as the separate buffers have the same overall functionality as a single buffer memory as per *In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965).

The examiner acknowledges the overall objective of the applicant's invention is to conserve hardware resources by providing a method to manage a single buffer with the multiple functional buffers existing in prior art.

7. Satterfield modified by the teachings of Lai as applied in claim 1 above, as per claim 2, Satterfield teaches a method comprising: while the input data is written into the buffer memory, changing (changing occurs via I/O pointers, Array #1 and #2 Pointers through RAPs to the respective ATT processors, changing applies to all the address values below accordingly, column 14, lines 21 – 44) the IO writing address in accordance with quantity of the input data (46a, column 22, lines 50 – 65); while the crypto engine reads the input data, changing the program reading address in accordance with quantity of the input data (47a, column 22, lines 50 – 65); while the result is written into the buffer memory, changing the program writing address in

accordance with quantity of the result (47b, column 22, lines 50 – 65); and while the buffer memory outputs the result, changing the IO reading address in accordance with quantity of the result (46b, column 22, lines 50 – 65).

8. Satterfield modified by the teachings of Lai as applied in claim 1 above, as per claim 3, Satterfield teaches a method comprising: defining a buffer end address in the buffer memory according to a data length request of the crypto engine processing the encryption algorithm or the decryption algorithm (initial values set at the end of the Parameters area section, column 14, lines 45 – 65), and dividing the buffer memory into an IO buffer area and a data storage area according to the buffer end address (BUFSEL column 13, lines 1 – 12, divides buffers into input and output and data storage area as shown in figure 1); storing the input data and the result in the IO buffer area (store result back to the user and output buffer, column 11, lines 48-59); and storing a cipher key in the data storage area, wherein the crypto engine utilizes the cipher key to process the encryption algorithm or the decryption algorithm (figure 4c depicts the data modification process which contains the XORn defined by the cipher used, column 7, lines 20 – 25).

9. Satterfield modified by the teachings of Lai as applied in claim 1 above, as per claim 4, Satterfield teaches a method comprising: while quantity of the input data stored between the IO writing address and the program reading address is smaller than a predetermined quantity, the crypto engine being controlled to suspend reading the input data beginning at the program reading address until quantity of the input data stored

between the IO writing address and the program reading address is larger than or equal to the predetermined quantity (suspending incrementing of ATTB only after the last ATT Block Entry has been used, column 15, lines 30 – 56).

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Applicant's Admitted Prior Art, AAPA is pertinent in regards to comprising the claimed I/O and program reading and writing addresses in order to properly handle the Input data, Cipher key and results.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571)272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

6/12/2006

AU 2181